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10/584,097	06/22/2006	Emmanuel Ardichvili	STW-FR030160US1	1408
25235 7590 08/19/2009 HOGAN & HARTSON LLP ONE TABOR CENTER, SUITE 1500			EXAMINER	
			DOAN, KIET M	
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,			2617	
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# Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentcolorado@hhlaw.com

### Application No. Applicant(s) 10/584,097 ARDICHVILI ET AL. Office Action Summary Examiner Art Unit KIET DOAN 2617 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 19 March 2009. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-21 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) 19-21 is/are allowed. 6) Claim(s) 1-3,5,6,10-12 and 14-16 is/are rejected. 7) Claim(s) 4-9,13,17 and 18 is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10)⊠ The drawing(s) filed on is/are: a)⊠ accepted or b)□ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some \* c) None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). \* See the attached detailed Office action for a list of the certified copies not received. Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date. Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/US)

Paper No(s)/Mail Date 03/24/09.

5) Notice of Informal Patent Application

6) Other:

Application/Control Number: 10/584,097 Page 2

Art Unit: 2617

### DETAILED ACTION

1. This office action is response to Applicant's Remarks file on 03/19/2009.

No claims are amended.

Claims 19 and 21 are new

#### Response to Arguments

Applicant's arguments filed 03/19/2009 have been fully considered but they are not persuasive.

In response to applicant's argument that prior art does not reject the claims concepts. The examiner disagrees for several reasons and notes that he must give each claim presented its broadest, reasonable interpretation.

1). Bolan clearly teaches the claims concepts such as the portable data module 120 that contain receiver chips 210, wherein the receiver chip 210 receives an RF signal from antenna and tracks/control the amplitude shifts of the RF signals to output a burst of pulse and since the base station sending variable duration pulse RF signal, the receiver chip 210 will tracks/controlling variable delay received signal (see Col.12, lines 20-34, Col.13, liens 55-65, Fig.8 Illustrate and described).

The examiner notice decoding and encoding are perform at converter chip 220.

2). Ishigaki put forward to cure the limitations of demodulation unit, wherein the demodulation unit for dispreading and demodulating a receiving RF signal of receiving signal and delay circuit that receiving separately/variable signal, detected and giving it a slot time delay (see Col.5, lines 38-50, Col. 6,lines 42-60).

Art Unit: 2617

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, in order to improve the control and arrangement channel signal without degradation or interference.

The examiner also reminds the applicant that the **recent landmark KSR** ruling puts forth that simple substitution of one known element or application for another to a piece of prior art ready for improvement is not patentable under 35 USC 103(a).

Accordingly, the claims are viewed as a combination that only unites elements with no change in respective functions of those elements and said combination yields predictable results.

Absent evidence that the modifications necessary to effect the combination of elements is <u>uniquely challenging or difficult for one of ordinary skill</u> the claims are also deemed unpatentable.

Art Unit: 2617

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

 Claims 1-3, 5, 6, 10, 11, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolan et al. (US 5,684,828) in view of Ishigaki et al. (US 4,977,578).

Consider claims 1 and 10. Bolan teaches a method of performing time drift compensation in a receiver, the method comprising the steps of:

receiving a signal, which comprises chips, at the receiver (Col.12, lines 20-21 teach receiver chip 210);

producing a control pulse after having received a certain number of chips of the received signal (Col.4, lines 47-56, Col.12, lines 25-34);

controlling a variable delay applied to the received signal (Col.13, lines 3-8, 56-67, Col.14, lines 1-2). Bolan fails to explicitly teach

sending, to demodulation units in the receiver, a delayed signal in which chips have been omitted or duplicated on the basis of said control pulse;

supplying, to said demodulation units in the receiver, a compensation signal that indicates whether chips have been omitted or duplicated in the delayed signal; and demodulating the delayed signal such that the demodulation units consider the omission or duplication of chips in the delayed signal.

Art Unit: 2617

In an analogous art, Ishigaki teaches

sending, to demodulation units in the receiver, a delayed signal in which chips have been omitted or duplicated on the basis of said control pulse (Col.5, lines 38-50, Col.10, lines 15-17):

supplying, to said demodulation units in the receiver, a compensation signal that indicates whether chips have been omitted or duplicated in the delayed signal; and demodulating the delayed signal such that the demodulation units consider the

omission or duplication of chips in the delayed signal (Col. 11, lines 60-64. Col.16, lines 4-50).

Therefore, it would have been obvious at the time that the invention was made to modify Bolan with Ishigaki's system such that receiver contain chips and pulse control for controlling a variable delay signal which chips have been omitted or duplicated in order to improve the control and arrangement channel signal without degradation or interference.

Consider claims 2 and 11. The combination of Bolan and Ishigaki teach the method according to claim 1. Further, Ishigaki teaches comprising the step of synchronizing the compensation signal to the control pulse (Col.3, lines 31-40, Col.4, lines 35-39).

Consider claim 3 and 12. The combination of Bolan and Ishigaki teach the method according to claim 1. Further, Bolan teaches comprising the step of aligning

Art Unit: 2617

said control pulse with a symbol boundary (Col.4, lines 47-56, Fig.5a-5b show as the aligning said control pulse with a symbol boundary).

Consider claims 5 and 14. The combination of Bolan and Ishigaki teach the method according to claim 1. Further, Ishigaki teaches wherein the compensation signal is given a first value which indicates that a chip has been omitted in the delayed signal and a second value which indicates that a chip has been duplicated in the delayed signal (Col. 11, lines 60-64, Col.16, lines 4-50).

Consider claims 6 and 15. The combination of Bolan and Ishigaki teach the method according to claim 1. Further, Ishigaki teaches wherein the step of demodulating chips comprises the steps of: descrambling the delayed chips; and despreading the descrambled chips (Abstract, lines 20-23, Col.2, lines 28-35).

 Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bolan et al. (US 5.684.828) in view of Ishiqaki et al. (US 4.977.578).

Consider claim 16. The combination of Bolan and Ishigaki teach the receiver according to claim 10, **but is silent on** wherein the demodulation units comprise: integrators arranged to integrate the demodulated pilot chips to create a pilot symbol and the demodulated data chips to create a data symbol.

In an analogous art, **Lundby teaches** wherein the demodulation units comprise: integrators arranged to integrate the demodulated pilot chips to create a pilot symbol

Art Unit: 2617

and the demodulated data chips to create a data symbol (Paragraph [0036-0037], [0033]).

Therefore, it would have been obvious at the time that the invention was made to modify Bolan and Ishigaki with Lundby's system such that integrators arranged to integrate the demodulated pilot chips to create a pilot symbol in order to provide multiple channel communication without interference.

## Allowable Subject Matter

Claims 19-21 are allow according to rewritten the independent in form including all of the limitations of the base claim and any intervening claims

Claims 4, 7-9, 13 and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2617

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KIET DOAN whose telephone number is (571)272-7863. The examiner can normally be reached on 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Appiah can be reached on 571-272-7904. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/584,097 Page 9

Art Unit: 2617

If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kiet Doan/ Examiner, Art Unit 2617

/Charles N. Appiah/ Supervisory Patent Examiner, Art Unit 2617